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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/430,192	10/29/1999	MICHAEL B. RAYNHAM	10981963-1	6908

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IP ADMINISTRATION
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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/430,192	RAYNHAM ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

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SUPERVISORY PATENT EXAMINER
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8/10/06

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Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on June 7, 2004, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options:

a. file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

b. initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

2. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Objections

3. Claim 6 is objected to because of the following informalities:

a. In claim 6, line 3, the acronym "IC" is introduced,

b. In claim 3, line 2, the acronym "LCD" is introduced, and

c. In claim 7, line 1, the acronym "LCD" is introduced.

4. Each time an acronym is introduced, the claims must clearly spell out the words represented by the acronym the first time the acronym is used. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. MPEP 608.01 states:

> *"I. TRADEMARKS*
> *The relationship between a trademark and the product it identifies is sometimes indefinite, uncertain, and arbitrary. The formula or characteristics of the product may change from time to time and yet it may continue to be sold under the same trademark. In patent specifications, every element or ingredient of the product should be set forth in positive, exact, intelligible language, so that there will be no uncertainty as to what is meant. Arbitrary trademarks which are liable to mean different things at the pleasure of manufacturers do not constitute such language. Ex Parte Kattwinkle, 12 USPQ 11 (Bd. App. 1931). However, if the product to which the trademark refers is set forth in such language that its identity is clear, the examiners are authorized to permit the use of the trademark if it is distinguished from common descriptive nouns by capitalization. If the trademark has a fixed and definite meaning, it constitutes sufficient identification unless some physical or chemical characteristic of the article or material is involved in the invention. In that event, as also in those cases where the trademark has no fixed and definite meaning, identification by scientific or other explanatory language is necessary. In re Gebauer-Fuelnegg, 121 F.2d 505, 50 USPQ 125 (CCPA 1941)."*

8. In this case, Applicant has attempted to use the trademark "i2c bus". Phillips has designed several different I2C busses since the early 1980's. There are many different I2C busses. It is uncertain to the examiner exactly what is meant by the term "i2c bus" since the term could be one of many different busses. Applicant must claim every element in a positive, exact and intelligible language, so that there will be no uncertainty

as to what is meant. For the purposes of examination, the term "i2c bus" will be interpreted as any known given bus. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2, 4, 6, 8, 9 and 10 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Uming U-Ming Ko, European Patent Application 0 419 105 A2 (herein after "Ko").

11. Referring to claim 1, Ko has taught a subsystem controller (Figure 1) implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components, the subsystem controller comprising:

a. a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality (column 4, line 22, figure 1, element 38);

b. a micro-controller that can execute software routines that implement control functionality (column 1, line 55-column 2, line 6, Figure 1, element 12);

c. read-only memory that stores executable code for execution by the micro-controller (column 2, lines 51-54, Figure 1, element 14);

d. random-access memory that can store data and executable code for execution by the micro-controller (column 2, line 55-column 3, line 3, Figure 1, element 16);

e. a bus interface for exchanging data and control signals between the subsystem controller and system processing components (abstract, Figure 1, column 3, line 53-column 4, line 4, column 4, lines 15-27, column 5, lines 2-11, column 9, lines 48-53, Figure 1, Any combination of at least elements 26, 34 and 28 is the claimed bus interface.); and

f. an additional electronic interface to a device (abstract, column 3, line 53-column 4, line 4, column 9, lines 48-53, At least element 28 is an interface to other integrated circuit chips. An integrated circuit chip is a device.) or subsystem controlled by the subsystem controller (Alternative claim language not required to read on the claim.).

12. Referring to claim 2, Ko has taught the subsystem controller of claim 1, as described above, and wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device (column 4, line 22, figure 1, element 38) and software routines executed by the micro-controller (column 1, line 55-column 2, line 6, Figure 1, element 12) (Hardware and software (instructions) are implemented in the controller.).

13. Referring to claim 4, Ko has taught the subsystem controller of claim 1, as described above, and wherein the bus interface is an I2C bus interface (abstract, Figure 1, column 3, line 53-column 4, line 4, column 4, lines 15-27, column 5, lines 2-11,

column 9, lines 48-53, Figure 1, Any combination of at least elements 26, 34 and 28 is the claimed bus interface.).

14. Referring to claim 6, Ko has taught a method for controlling a subsystem within a complex electrical device, the method comprising:

a. providing a single-IC subsystem controller (Figure 1);

b. programming control functionality into the single-IC subsystem controller by programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller (column 4, line 22, figure 1, element 38),

c. implementing software routines for execution by a micro-controller within the single-IC subsystem controller (column 2, lines 51-54, Figure 1, element 14), and

d. storing the software routines in the single-IC subsystem controller (column 2, line 55-column 3, line 3, Figure 1, element 16); and

e. interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device (abstract, Figure 1, column 3, line 53-column 4, line 4, column 4, lines 15-27, column 5, lines 2-11, column 9, lines 48-53, Figure 1, Any combination of at least elements 26, 34 and 28 perform the claimed interconnecting at least one subsystem.).

15. Referring to claim 8, Ko has taught the method of claim 6, as described above, and wherein the complex electrical device is a computer system (abstract, The invention of Ko is a system of integrated circuits that process information to produce results, which is a computer system.).

16. Referring to claim 9, Ko has taught the method of claim 6, as described above, and wherein the single-IC subsystem controller includes the complex programmable logic device, the micro-controller, a read-only memory, a random access memory, a bus interface, and an additional electronic interface (Figure 1,abstract).

17. Referring to claim 10, Ko has taught the method of claim 9, as described above, and wherein interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface (abstract, column 3, line 53-column 4, line 4, At least element 28 interconnects the subsystem controller (Figure 1) to the subsystem. The subsystem is at least for example other integrated circuit chips.).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uming U-Ming Ko, European Patent Application 0 419 105 A2 (herein after "Ko") in view of Alexander, US Patent 5,953,684 (herein after "Alexander").

20. Referring to claim 3, Ko has taught the subsystem controller of claim 1, as described above, Ko has not specifically taught that the subsystem controller is programmed to control display of information on an LCD display window included in an external front panel display of a server computer. However, Ko has taught that it is

desirable to test the circuit states of the digital signal processor (abstract, column 5, lines 28-44). Ko has not specifically taught the details of the test equipment circuitry connected to the test pin that actually tests and controls the subsystem controller. Alexander has taught test equipment that is used to acquire test data via a data path (Alexander, column 3, lines 43-45). The test equipment includes an LCD for displaying acquired test data and an input means (such as a keypad) for dynamically inputting data and parameters to configure and operate the test equipment based on the data output from the LCD (Alexander, column 3, lines 43-45, column 5, line 58-column 6, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the subsystem controller be programmed to control display of information on an LCD display window included in an external front panel display of a server computer, for the desirable purpose of allowing an end user to run dynamic tests on the system.

21. Referring to claim 7, Ko has taught the method of claim 6, as described above. Ko has not specifically taught wherein the subsystem is an LCD display window that displays information about the components within the complex electrical device and about the state of the complex electrical device. However, Ko has taught that it is desirable to test the circuit states of the digital signal processor (abstract, column 5, lines 28-44). Ko has not specifically taught the details of the test equipment circuitry connected to the test pin that actually tests and controls the subsystem controller. Alexander has taught test equipment that is used to acquire test data via a data path (Alexander, column 3, lines 43-45). The test equipment includes an LCD for displaying

acquired test data and an input means (such as a keypad) for dynamically inputting data and parameters to configure and operate the test equipment based on the data output from the LCD (Alexander, column 3, lines 43-45, column 5, line 58-column 6, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the subsystem of Ko be an LCD display window that displays information about the components within the complex electrical device and about the state of the complex electrical device, as taught by Alexander, for the desirable purpose of allowing the user to run dynamic tests on the system.

22. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uming U-Ming Ko, European Patent Application 0 419 105 A2 (herein after "Ko").

23. Referring to claim 5, Ko has taught the subsystem controller of claim 1, as described above. Ko has not specifically taught wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines. However, Ko has taught that data is stored in the RAM in a 16-bit format (Ko, column 3, lines 35-45). Having the input/output interface be at least 16 bits would have allowed for the interface to easily output the system data to other devices such that the data read would only require one read step on the interface. Furthermore, it has been held that changing the size is not accorded patentable weight, see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the additional electronic interface of Ko, be any size bus, such as an 8-bit input/output bus and additional signal lines (a 16-bit bus is 8 bits and 8 additional signal bit lines), as it has been held that changing the

size is not a patentable difference and that having the bus be a 16-bit bus would ease transferring data through the interface.

Response to Arguments

24. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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8/18/2006